

Notice of References Cited	Application/Control No. 10/720,562		Applicant(s)/Patent Under Reexamination CORREALE ET AL.	
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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,517,132	05-1996	Ohara, Kazutake	326/41
*	B	US-5,990,706	11-1999	Matsumoto et al.	326/98
*	C	US-6,167,554	12-2000	Ishikawa et al.	716/1
*	D	US-6,266,798	07-2001	Kanazawa et al.	716/4
*	E	US-6,941,534	09-2005	Fukasawa, Shinji	716/8
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	CHEN et al., "On Gate Level Power Optimization Using Dual-Supply Voltages," IEEE Trans. on VLSI Systems, Vol. 9, No. 5, October 2001, pages 616-629
	V	HAMADA et al., "A Top-Down Low Power Design Technique Using Clustered Voltage Scaling with Variable Supply-Voltage Scheme," IEEE 1998 Custom ICs Conference, pages 495-498.
	W	IGARASHI et al., "A Low-power Design Method Using Multiple Supply Voltages," 1997 ACM, pages 36-41.
	X	ISHIHARA et al., "Level Conversion for Dual-Supply Systems," ISLPED '03, August 25-27, 2003, pages 164-167.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	KANG et al., "Multiple-Vdd Scheduling/Allocation for Partitioned Floorplan," Proc. of the 21 st Int'l Conference on Computer Design, 2003, 7 pages.
	V	PANGJUN et al., "Clock Distribution Using Multiple Voltages," ISLPED99, ACM 1999, pages 145-150.
	W	USAMI et al., "Low-power Design Methodology and Applications utilizing Dual Supply Voltages," 2000 IEEE, pages 123-128.
	X	YEH et al., "Layout Techniques Supporting the Use of Dual Supply Voltages for Cell-Based Designs," 1999 ACM Design Automation Conference, 6 pages.

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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.